REMARKS

The present case was originally filed 11/26/2001 with five claims. Claims 1-5 currently stand rejected by the Examiner under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that applicants regard as their invention. Furthermore, the abstract, parts of the disclosure, and Figure 14 were objected to.

In response, Applicants have amended the abstract, the disclosure, Figure 14 and Claims 1 and 3-5. Applicants have also added new claims 6-12. Thus Claims 1-12 are now being presented for further examination.

Objection to the Abstract and the Disclosure

The abstract and disclosure have been amended in accordance with the direction provided by the Examiner. Several other minor oversights have also been corrected.

Objection to Figure 14

Figure 14 was objected to because Figure 14c was mislabeled as "12c". A corrected Figure 14 is attached. Also attached is a marked-up copy of the original illustrating the foregoing change to Figure 14 in red ink; and a letter to the Official Draftsperson requesting the replacement of the original Figure 14 with the corrected Figure 14.

Rejection under 35 U.S.C. §112, second paragraph

Claims 1-5 as originally submitted were rejected as being indefinite for failing to particularly point out and distinctly claim the subject matter that applicants regard as their invention. The applicants respectfully submit that the rejection has been overcome in view of their amendments.

In particular, Claim 1 was identified as being vague and indefinite where "one or more analog-to digital converters" (line 7) is claimed as being coupled to a "plurality of digital programmable switching devices" (line 4). The Examiner

queries whether the "plurality of digital programmable switching devices" provides analog results and has concern that the applicants present an incomplete claim. The same concern was expressed in conjunction with Claim 4, where the applicants recite that both "digital-to-analog" and "analog-to-digital" converters are coupled to a field programmable interconnect device ("FPID"). The Examiner asks whether the FPID provides both digital and analog results.

Starting at page 1, last paragraph, and continuing through page 2, the applicants explain that MOSFET devices, such as FPIDs, exhibit some resistance. The applicants have found that an FPID actually behaves more like a resistor, which the applicants state is "a fact very important to the principle behind the present invention." Typically, FPIDs exhibit resistive values in the range of 50 ohms to 500 ohms, based on switch design and process technology. What those skilled in the electrical art typically view as unwanted signal deterioration and design complexity associated with FPIDs, precludes this type of switch from being used in most analog applications.

With the current invention, however, the parasitic resistance associated with FPIDs is harnessed through their use in a resistive network, as claimed by the applicants. More particularly, the applicants' claimed invention is used as a linear equation solver using the finite difference method. It should be apparent to those skilled in the art that a computer can be programmed to process the equations provided by the applicants in pages 2 through 5 of their specification. The applicants' invention primarily lies in using voltage differential inputs from a resistive network to generate the signals utilized by the computer to solve a differential equation.

The terms "may be" (line 12) and "can inject" (line 9) were said to be indefinite in the office action. The applicants have amended Claims 1 and 4 to replace these terms with more definite language.

With respect to claim 5, Examiner states that the necessary detailed steps or physical structure to adequately describe and constitute the proposed method

are not recited. In response, the applicants have amended claim 5 to read as follows, to more clearly define the claimed invention:

> 5. (currently amended) A method of solving problems having a partial differential equation by the finite difference method using a programmable resistive grid including a network of field programmable interconnect devices (FPIDs), said programmable resistive grid having externally accessible pins and grid nodal points, comprised of:
>
> impressing voltages from an analog voltage source onto said externally accessible pins, said voltages corresponding to Dirichlet boundary conditions;
>
> measuring the voltages at grid nodal points; and
>
> providing voltage measurements from the grid nodal points to a computer, wherein the computer is programmed to use the voltage measurements to solve the partial differential equation.

Additionally, the applicants are submitting new Claims 6-12, which depend from Claim 5. Claims 6-12 present additional aspects of novelty described in the original specification, and are believed to be allowable based on a favorable determination of Claim 5. No further search is required by the addition of Claims 6-12.

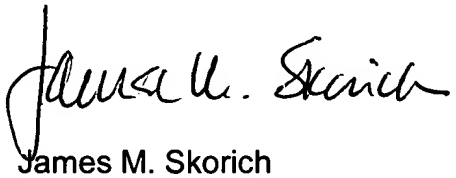
The applicants believe that their claims, both those presently amended as well as added, are supported by the specification. The applicants contend that their claims as amended now overcome the rejection and, therefore, merit reconsideration and allowance.

Conclusion

In view of the foregoing remarks, the applicants submit the specification and drawings have been amended to overcome the cited objections; that Claims 1-5 have been placed in allowable form; and that new Claims 6-12 are also allowable. Accordingly, the applicants earnestly solicit the favorable consideration of their application, and respectfully request that it be passed to issuance in its amended form.

Should the Examiner discern any remaining impediment to the prompt allowance of the aforementioned claims that might be resolved or overcome with the aid a telephone conference, he is cordially invited to call the undersigned at the telephone number set out below.

Respectfully submitted,



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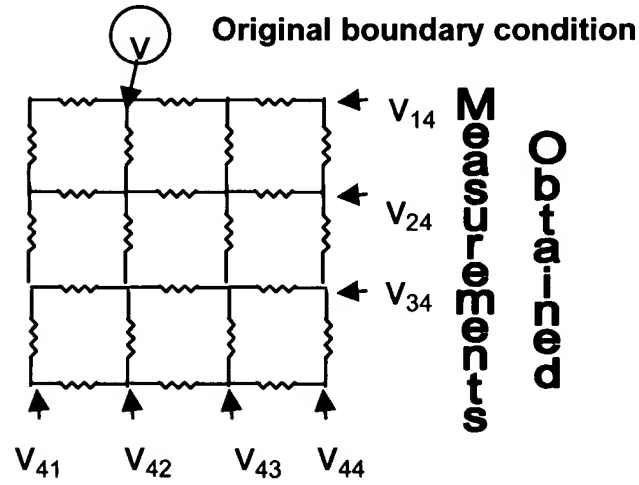
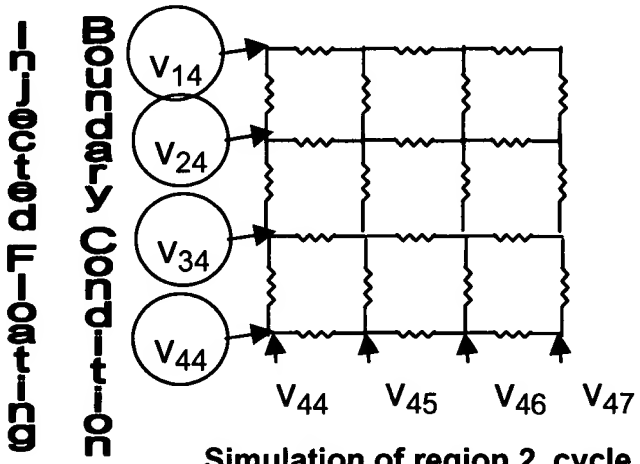


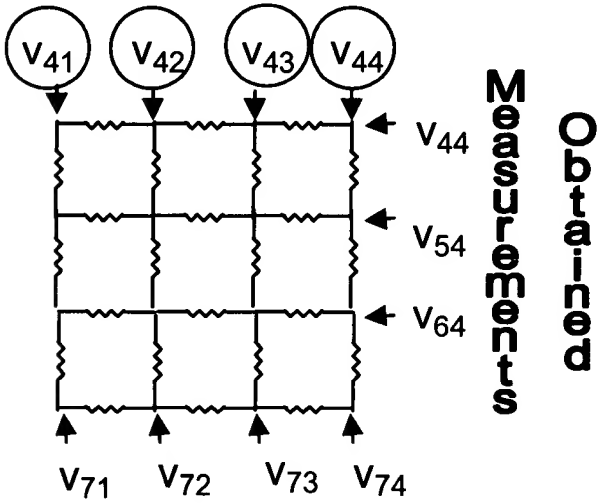
Simulation of region 1, cycle 1

14a



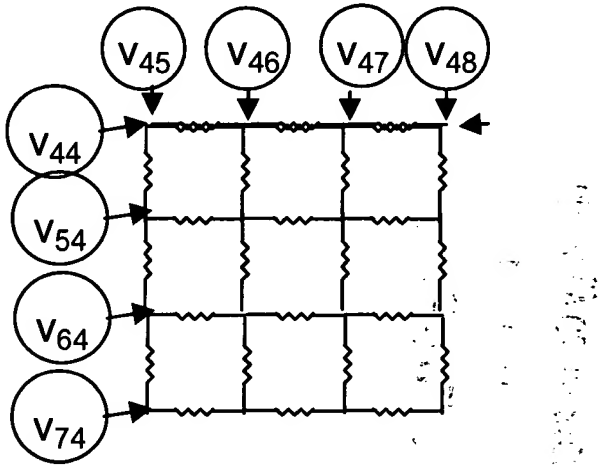
Simulation of region 2, cycle 1

14b



Simulation of region 3, cycle 1 14c

~~12c~~



Simulation of region 4, cycle 1

14d

FIG. 14